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10/826,366	04/19/2004	Hiroshi Sera	119209	1035

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EXAMINER	
RODGERS, COLLEEN E	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/826,366	SERA, HIROSHI	
	Examiner	Art Unit	
	Colleen E. Rodgers	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Amendment filed 28 March 2006. By this amendment, claims 1, 4, 5 and 9-11 are amended. Claims 1-12 remain pending.

Claim Objections

2. Claim 5 is objected to because of the following informalities: in both lines 19 and 22, remove the word "at" for proper grammar. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 6 and 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al** (US Patent Application Publication 2002/0145142).

Regarding claims 1 and 10, **Chen et al** teaches a method of forming a thin-film semiconductor device, the method including the steps of:

forming a semiconductor film **32** with a predetermined pattern on a substrate **30**;

forming a gate-insulating film **34** on the semiconductor film **32**;

forming a tapered gate electrode **36** [see paragraph 0019, wherein it is noted that the gate electrode may be trapezoidal rather than rectangular] on the gate-insulating film **34**;

implanting a low concentration of impurity into the substrate **30** through the gate electrode **36** functioning as a mask [see paragraph 0020];

forming a layered insulating film composed of at least two different insulating films **40, 42** on the gate electrode **36** on the substrate **30**;

etching an entire surface of the layered insulating film to form a predetermined pattern in at least one of the layers **42** of the layered insulating film, the predetermined pattern having a width greater than a width of the gate electrode **36** and smaller than a width of the substrate **30** [see Fig. 2D]; and

implanting a high concentration of impurity through the layered insulating film formed according to a predetermined pattern functioning as a mask [see paragraph 0021].

Chen et al does not disclose that the gate electrode is tapered at a 20° to 80° angle. These claims are *prima facie* obvious without a showing that the claimed angles achieve unexpected results relative to the prior art angles. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art in general conditions is obvious). In this case, there exists no evidence of record that the angle of tapering provides unexpected results in the gate electrode produced. One of ordinary skill in the art would be motivated to optimize the taper angle to provide for device performance.

Regarding claim 2, **Chen et al** discloses the method of claim 1 as described above, wherein the uppermost layer **42** of the layered insulating film is isotropically formed and anisotropically etched [see Figs. 2C and 2D].

Regarding claim 3, **Chen et al** discloses the method of claim 2 as described above, wherein anisotropic etching is performed after the formation of the predetermined pattern as shown in Fig. 2D, the predetermined pattern having a width greater than the width of the gate electrode **36** and smaller than the width of the semiconductor film **32** [see Fig. 2E].

Regarding claim 6, **Chen et al** discloses the method of claim 1 as described above, wherein the etching rate of the upper insulating layer is greater than the etching rate of the lower insulating layer in the first, dry-etching process (etch-selective to the uppermost insulating layer), and the etching rate of the exposed lower insulating layer is greater than the etching rate of the remaining upper insulating layer in the second, wet-etching process (etch-selective to the lower insulating layer). As best understood, it is inherent that in a process utilizing two etch steps, etch selectivity is practiced to control which material is etched by each process.

Regarding claims 9 and 11, **Chen et al** discloses the method of claims 1 and 10 as described above. **Chen et al** furthermore discloses that the insulating film **40** is formed at least along the sides of the gate electrode **36** [see Figs. 2C-2F], and each of the source region and the drain region **48** of the semiconductor **32** have a low-concentration region **38** corresponding to a portion of the insulating film **40** with a width greater than the width of the gate electrode **36** [see Fig. 2F].

Regarding claim 12, **Chen et al** discloses the method of claim 11 as described above, wherein the resulting electro-optic apparatus may be included in an LCD display, which is an electronic apparatus [see paragraph 0004].

5. Claims 4, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al** (US Patent Application Publication 2002/0145142 A1) in view of **Tsubone** (USPN 5,100,820).

Regarding claims 4, **Chen et al** teaches a method of forming a thin-film semiconductor device, the method including the steps of:

forming a semiconductor film **32** with a predetermined pattern on a substrate **30**;

forming a gate-insulating film **34** on the semiconductor film **32**;

forming a tapered gate electrode **36** [see paragraph 0019, wherein it is noted that the gate electrode may be trapezoidal rather than rectangular] on the gate-insulating film **34**;

implanting a low concentration of impurity into the substrate **30** through the gate electrode **36** functioning as a mask [see paragraph 0020];

forming a layered insulating film composed of at least two different insulating films **40, 42** on the gate electrode **36** on the substrate **30**;

etching an entire surface of the layered insulating film to form a predetermined pattern in at least one of the layers **42** of the layered insulating film, the predetermined pattern having a width greater than a width of the gate electrode **36** and smaller than a width of the substrate **30** [see Fig. 2D]; and

implanting a high concentration of impurity through the layered insulating film formed according to a predetermined pattern functioning as a mask [see paragraph 0021].

Chen et al does not disclose what material is used to form the gate-insulating layer **34**; therefore, **Chen et al** does not disclose that the uppermost insulating layer and the gate-insulating layer have substantially the same composition. **Tsubone** teaches substantially the method of **Chen et al** with the exception of the semiconductor layer. Furthermore, **Tsubone** teaches that the gate-insulating film **53** and the uppermost insulating layer **60** of the layered insulating film have

substantially the same composition [see col. 7, lines 61-68 and col. 8, lines 64-66]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the materials of **Tsubone** in the method of **Chen et al** because the materials of **Tsubone** are art-recognized materials for use in insulating layers.

Regarding claim 7, the prior art **Chen et al** discloses the method of claim 1 as described above. **Chen et al** does not disclose that the gate-insulating film is composed of silicon oxide. **Tsubone** teaches substantially the method of **Chen et al** with the exception of the semiconductor layer. Furthermore, **Tsubone** teaches that the gate-insulating film is composed of silicon oxide [see col. 7, lines 61-68]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the materials of **Tsubone** in the method of **Chen et al** because silicon oxide is an art-recognized material for use in insulating layers.

Regarding claim 8, the prior art **Chen et al** discloses the method of claim 7 as described above. **Chen et al** does not disclose that the first insulating layer is silicon nitride and the second insulating layer is silicon oxide. **Tsubone** teaches substantially the method of **Chen et al** with the exception of the semiconductor layer. Furthermore, **Tsubone** teaches that the first insulating layer **56** is silicon nitride [see col. 8, lines 10-15] and the second insulating layer **60** is silicon oxide [see col. 8, lines 64-66]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the materials of **Tsubone** in the method of **Chen et al** because silicon oxide and silicon nitride are art-recognized materials for use in insulating layers.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen et al** (US Patent Application Publication 2002/0145142) in view of **Sonderman et al** (USPN 6,660,539). **Chen et al** teaches a method of forming a thin-film semiconductor device, the method including the steps of:

forming a semiconductor film **32** with a predetermined pattern on a substrate **30**;

forming a gate-insulating film **34** on the semiconductor film **32**;

forming a tapered gate electrode **36** [see paragraph 0019, wherein it is noted that the gate electrode may be trapezoidal rather than rectangular] on the gate-insulating film **34**;

implanting a low concentration of impurity into the substrate **30** through the gate electrode **36** functioning as a mask [see paragraph 0020];

forming a layered insulating film composed of at least two different insulating films **40, 42** on the gate electrode **36** on the substrate **30**;

etching an entire surface of the layered insulating film to form a predetermined pattern in at least one of the layers **42** of the layered insulating film, the predetermined pattern having a width greater than a width of the gate electrode **36** and smaller than a width of the substrate **30** [see Fig. 2D]; and

implanting a high concentration of impurity through the layered insulating film formed according to a predetermined pattern functioning as a mask [see paragraph 0021].

Chen et al does not disclose that the etching is controlled via endpoint detection. However, **Sonderman et al** teaches that endpoint detection is utilized in etching processes [see col. 2, lines 17-24]. It would have been obvious to one of ordinary skill in the art at the time of invention to employ an endpoint detection process as taught by **Sonderman et al** in the method of **Chen et al** in order to prevent either under- or over-etching of the insulating film.

Response to Arguments

6. Applicant's arguments with respect to claims 1-3, 5, 6 and 10-12 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's arguments filed 28 March 2006 with respect to claims 4, 7 and 8 have been fully considered but they are not persuasive. Applicant alleges that layer **60** of **Tsubone** is not part of the configuration that includes a gate-insulating film, a first insulating layer and a second insulating layer. Applicant asserts that since "layers" **53** and **60** are separated by the gate electrode **56**, they cannot be first and second insulating layers as instantly claimed. Examiner agrees with this interpretation of the reference; in fact, oxide **53** is the gate-insulating film, nitride **56** is the first insulating film, and oxide **60** is the second insulating film. Therefore, layer **60** is a second insulating film, and is formed of substantially the same composition as the gate-insulating film **53**.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen E. Rodgers whose telephone number is (571) 272-8603. The examiner can normally be reached on Monday through Friday, 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CER

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